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UNITED STATES DISTRICT COURT
NORTHERN DISTRICT OF CALIFORNIA
SAN FRANCISCO DIVISION

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|---|---|
| RICOH COMPANY, LTD.,<br><br>Plaintiff,<br><br>vs.<br><br>AEROFLEX INCORPORATED, et al.,<br><br>Defendants. | **CASE NO. C-03-4669-MJJ (EMC)** |
| SYNOPSYS, INC.,<br><br>Plaintiff,<br><br>vs.<br><br>RICOH COMPANY, LTD.,<br><br>Defendant. | **CASE NO. C-03-2289-MJJ (EMC)**<br><br>**RICOH'S CLAIM CONSTRUCTION OPENING BRIEF**<br><br>**Date: October 20, 2004**<br>**Time: 2:30 p.m.**<br>**Courtroom: 11** |

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## I. INTRODUCTION

Now before the Court in this matter is the claim construction of claims 13-17 of U.S. Patent No. 4,922,432 ("the '432 patent") (RCL002929-54) (attached as Exhibit No. 1).[1] Claims 13-17 are directed to a process for the design and production of application specific integrated circuits ("ASICs").

This matter is centered around the infringement of the '432 patent by Aeroflex, Inc. and Aeroflex Colorado Springs, Inc. (collectively "Aeroflex"); AMI Semiconductor, Inc.; and Matrox Graphics, Inc., Matrox Tech, Inc., Matrox Electronic Systems, Ltd., and Matrox International Corp. (collectively "Matrox"); all of these parties are referred to as "the ASIC Defendants." Ricoh Company, Ltd. ("Ricoh") alleges that the ASIC Defendants infringe claims 13-17 of the '432 patent based primarily on their use of certain software products provided by Synopsys, Inc. ("Synopsys") and the ASIC Defendants' own independent decisions relating to the design and manufacture of ASICs. (For simplification, the ASIC Defendants and Synopsys will be collectively referred to herein as "Defendants.")

Ricoh proposes a construction of claims 13-17 of the '432 patent that is based on the ordinary and customary meaning of the claim language consistent with the public record of the '432 patent (i.e., claims, specification, and file history). The public record of the '432 patent is unambiguous in describing the scope of claims 13-17, and thus, there is no need to consider or rely on extrinsic evidence to properly construe the claims.

Defendants, on the other hand, propose to narrowly confine the scope of the claims in a manner that is inconsistent with the well-established law of claim construction. They repeatedly propose constructions that would restrict the claims to exemplary embodiments detailed in the '432 patent, or that would impose new limitations on the claims that appear framed simply to support their non-infringement theories for use later at trial. As shown below,

[1] All of the exhibits referred to herein are attached to the Declaration of Eric Oliver in Support of Ricoh's Claim Construction Opening Brief, which is filed simultaneously herewith.

these positions are inconsistent with the public record of the '432 patent and the application of the relevant law.

## II. PROCEDURAL BACKGROUND

By the Order dated July 22, 2004, the Court has explicitly indicated that no extrinsic evidence should be introduced or relied on for this claim construction proceeding. See Vitronics Corp. v. Conceptronic, Inc., 90 F.3d 1576, 1583 (Fed. Cir. 1996) (attached as Exhibit C1) ("[W]here the public record unambiguously describes the scope of the patented invention, reliance on any extrinsic evidence is improper."). Nevertheless, Defendants' positions (as set forth in Exhibit A of the Joint Claim Construction And Prehearing Statement filed July 16, 2004 ("JCC Statement") (JCC Statement Exhibit A attached as Exhibit No. 2)) are heavily dependent on extrinsic evidence, particularly the Declaration of their expert Dr. Thaddeus J. Kowalski. Although Defendants repeatedly attempt to inject extrinsic evidence into their claim construction arguments, this effort is inconsistent with the Court's clear direction as well as Vitronics. In this brief, Ricoh has not attempted to address Defendants' extrinsic evidence. Ricoh maintains that the Court need not ever consider such extrinsic evidence because the public record in this case is unambiguous with respect to the claim language of claims 13-17 of the '432 patent.

## III. FACTUAL BACKGROUND[2]

The '432 patent's subject matter was the joint conception of Mr. Hideaki Kobayashi of International Chip Corporation ("ICC") and Mr. Masahiro Shindo of Ricoh. The patent was filed in 1988 and issued in 1990. During this period, the patent was jointly owned by Ricoh and ICC. Ultimately, ICC was renamed Knowledge Based Silicon Corporation ("KBSC"). In 2001,

[2] Should the Court deem it necessary, Ricoh is prepared to provide a Declaration or other evidence supporting any facts provided in this Factual Background Section.

KBSC assigned its legal interest in the '432 patent to Ricoh, making Ricoh the sole owner of the patent.

Ricoh conducts global-scale activities including development, production, marketing, after-sales service, and recycling of office equipment, including copiers and printers, information technology equipment, optical devices, and other electronic equipment in regions around the world. As part of these activities, Ricoh manufactures ASICs for use in a variety of products. Ricoh's involvement in ASIC manufacturing is what in large part led to its joint effort with ICC to develop an improved process for designing and producing ASICs. The innovative nature of Ricoh and ICC's efforts was recognized by the United States Patent and Trademark Office, prompting the issuance of the '432 patent.

The ASIC design process at issue here is used as part of the overall process of manufacturing ASICs. ASICs are used in products for a variety of applications, such as in consumer products (e.g., cell phones, digital cameras, and other video equipment), communications and electronic data processing products, industrial products (e.g., in applications involving electrical noise, and high voltage applications), aerospace and defense products, medical imaging products, automotive products, and many other products that require integrated circuits designed to perform a specific function.

At the beginning of the manufacturing process, ASICs are often created by a design team, in which each designer (or each group of designers) designs a designated section of the ASIC. This effort involves the designer describing tasks that the ASIC is to perform. Often, the designer's description is called a "specification." When produced, the ASIC described in the specification is made up of a multitude of interconnected hardware cells used to perform the functions required of the ASIC. The process of selecting these hardware cells based on the designer's specification is called "synthesis." The '432 patent is directed to an improved process for synthesizing ASICs.

Historically, as part of the design phase of the manufacturing process, highly skilled design engineers, having specialized knowledge of very large scale integration ("VLSI"), would

create structural level design specifications that defined the various hardware components required to perform the desired functions of the ASIC. These types of design specifications can be referred to as "architecture dependent" design specifications because they set out a definite structure that is used in the specification itself. The creation of these architecture dependent design specifications required extensive knowledge of the various hardware components that were to make up the ASIC, as well as details of the implementation (e.g., interconnection requirements, signal level compatibility, timing compatibility, and physical layout of hardware components). Describing ASICs at the structural level not only was time-consuming and expensive, but provided limited flexibility in the design process and required a designer who has specialized VLSI knowledge. These shortcomings were incompatible with the rising commercial demand for more complex ASICs having increased numbers of components and faster time to market requirements.

One way of meeting some of these rising market demands was to simplify the design phase of the process so that those without specialized skill in VLSI design could more readily design the ASICs. In accomplishing this, the patentee recognized that it was important both to raise the level of abstraction of the ASIC input specifications and to develop computer aided design ("CAD") systems for receiving such input specifications and selecting hardware cells to be used in the ASICs. Specifically, the process needed to be one where the input specification did not require traditional, architecture dependent descriptions (e.g., structural flowcharts, Boolean equations, etc.).[3] The associated CAD system needed to be one that could receive the desired higher level input descriptions and that could synthesize these descriptions to architecture dependent hardware cells to lead to the production of the ASIC.

[3] "Structural flowcharts" describe the flow of information between structures in a circuit. "Boolean equations" describe a logical combinatorial system (as Boolean algebra) that represents symbolically relationships (as those implied by the logical operators AND, OR, and NOT) between entities (as sets, propositions, or on-off computer circuit elements, etc.).

The invention recited in claims 1-20 of the '432 patent is the culmination of the patentee's efforts to meet these needs. It enables the use of higher level input descriptions by allowing designers to describe ASIC specifications at a functional level. This functional level is done without specification of structure, implementing technology or architecture (i.e., an "architecture independent" level). The unique process also provides a novel process of taking such architecture independent specifications and selecting previously designed circuit components or structure used as building blocks for implementing in an ASIC (i.e., "hardware cells"). The process selects the optimum hardware cells to be included in the desired ASIC. In this way, even a user who does not have expertise in VLSI design can write architecture independent ASIC descriptions that ultimately can result in the automatic selection of hardware cells to be used in the ASIC.

The utilization of various aspects of the innovative process of the '432 patent has simplified and sped up the process of manufacturing ASICs. The '432 patent's novel method not only has opened up the process to designers who do not have the expertise in VLSI design, but also has led to a more efficient, cost-effective, and flexible process for the design and production of the ASICs.

The claims at issue in this proceeding are claims 13-17. As will be described in more detail below, independent claim 13 is directed to a process in which a designer describes an ASIC through an input specification using architecture independent descriptions. These architecture independent descriptions are used to select architecture dependent hardware cells. This process uses a library of definitions of the architecture independent, functional descriptions, a library of available hardware cells, and a storehouse of expert know-how or knowledge (referred to as a "knowledge base," which is a database embodying the knowledge of VLSI experts in the form of "rules"). In particular, for each desired function to be performed by the ASIC, one of the definitions from the library of definitions is specified. The rules in the knowledge base are then applied to select architecture dependent hardware cells from the library of available hardware cells.

Dependent claims 14-17 are directed to the same design process recited in claim 13. Dependent claim 14, however, adds a process step of generating mask data used to produce the ASIC designed using the process. Dependent claim 15 adds a process step of generating signal lines for carrying data ("data paths") between hardware cells selected for use in the designed ASIC. Dependent claim 16 clarifies that the step added by claim 15 is performed using rules in a knowledge base. Dependent claim 17 adds a step of generating signal lines for carrying control signals to hardware cells selected for use in the designed ASIC.

Because claims 1-12 and 18-20 contain significant limitations not found in the broader claims 13-17, Ricoh has not asserted them in its infringement action against the ASIC Defendants. Although not at issue here, claims 1-12 and 18-20 are summarized as follows for the convenience of the Court.

Claims 1-8 are directed to a computer-aided design system that enumerates exemplary tools that can be used to perform an ASIC design process similar to that described above. The claims provide, for example, a macro library defining architecture independent functions that may be desired in the ASIC to be produced, a cell library defining available hardware cells that can be used in the ASIC to be produced, and an expert system that includes a knowledge base containing rules for selecting hardware cells and an inference engine for selecting cells based on rules in the knowledge base. Claims 9-12 are also directed to a computer-aided design system similar to that described in claims 1-8. Claims 9-12, however, restrict the system to use of a flowchart editor that can be used to create a flowchart representation of the architecture independent functions desired in the ASIC to be produced. Claims 18-20 are directed to a design process for designing ASICs similar to that in claims 13-17. Claims 18-20, however, restrict the claim process to use of a flowchart description of the architecture independent functions desired in the ASIC to be produced.

## IV. LEGAL STANDARD

The construction of a patent claim is a matter of law for the Court. Markman v. Westview Instruments, Inc., 517 U.S. 370, 372 (1996) (attached as Exhibit C2). To determine the meaning of a patent claim, the Court considers three sources: the claims, the specification, and the prosecution history. Markman v. Westview Instruments, Inc., 52 F.3d 967, 979 (Fed. Cir. 1995) (en banc) (attached as Exhibit C3), aff'd, 517 U.S. 370 (1996).

First, the Court looks at the words of the claims. Vitronics, 90 F.3d at 1582. "[T]he analytical focus must begin and remain centered on the language of the claims themselves, for it is that language that the patentee chose to use to particularly point[ ] out and distinctly claim[ ] the subject matter which the patentee regards as his invention." Tex. Digital Sys., Inc. v. Telegenix, Inc., 308 F.3d 1193, 1201-02 (Fed. Cir. 2002) (attached as Exhibit C4) (internal quotation marks and citations omitted) (alterations in original), cert. denied, 538 U.S. 1058 (2003). Thus, there is a "heavy presumption" that claim terms bear their ordinary meaning, as understood by persons skilled in the relevant art. Id. at 1202; see also Teleflex, Inc. v. Ficosa N. Am. Corp., 299 F.3d 1313, 1325 (Fed. Cir. 2002) (attached as Exhibit C5).

Second, it is always necessary to review the specification to determine if the presumption of the ordinary meaning is rebutted. Tex. Digital Sys., 308 F.3d at 1204. The presumption is only rebutted in situations where the inventor: (1) acting as his or her own lexicographer, has clearly set forth an "explicit definition" of the term that is different from its ordinary meaning; or (2) has disavowed or disclaimed scope of coverage by using words of "manifest exclusion or restriction." Id.

> But if the meaning of the words themselves would not have been understood to persons of skill in the art to be limited only to the examples or embodiments described in the specification, reading the words in such a confined way would mandate the wrong result and would violate our proscription of not reading limitations from the specification into the claims.

Id. at 1205; see also Teleflex, 299 F.3d at 1326 ("limitations from the specification are not to be read into the claims").

Third, the Court may consider the prosecution history of the patent, if in evidence. Vitronics, 90 F.3d at 1582. "Although the prosecution history can and should be used to understand the language used in the claims, it . . . cannot enlarge, diminish, or vary the limitations in the claims." Markman, 52 F.3d at 980 (internal quotation marks and citations omitted); see also Golight, Inc. v. Wal-Mart Stores, Inc., 355 F.3d 1327, 1332 (Fed. Cir. 2004) (attached as Exhibit C6) ("Because the statements in the prosecution history are subject to multiple reasonable interpretations, they do not constitute a clear and unmistakable departure from the ordinary meaning of the [claim term at issue]."); Sunrace Roots Enter. Co. v. SRAM Corp., 336 F.3d 1298, 1306 (Fed. Cir. 2003) (attached as Exhibit C7) ("To be given effect, such a disclaimer must be 'clear and unmistakable.'" (quoting Omega Eng'g, Inc. v. Raytek Corp., 334 F.3d 1314, 1325 (Fed. Cir. 2003))) (attached as Exhibit C8).

Ordinarily, the Court should not rely on expert testimony to assist in claim construction, because the public is entitled to rely on the public record of the patentee's claim (as contained in the patent claim, the specification, and the prosecution history) to ascertain the scope of the claimed invention. Vitronics, 90 F.3d at 1583. "[W]here the public record unambiguously describes the scope of the patented invention, reliance on any extrinsic evidence is improper." Id. Extrinsic evidence should be used only if needed to assist in determining the meaning or scope of technical terms in the claims, and may not be used to vary or contradict the terms of the claims. Id. (quoting Pall Corp. v. Micron Separations, Inc., 66 F.3d 1211, 1216 (Fed. Cir. 1995) (attached as Exhibit C9)); Markman, 52 F.3d at 981. However, the Court is free to consult reference materials, such as dictionaries, for assistance in determining the ordinary meaning of a claim term and such sources are not considered extrinsic evidence. Tex. Digital Sys., 308 F.3d at 1202-03. Further, the intrinsic record must be consulted to determine which definition is most consistent with the use of the word by the inventor. Id. at 1203. "If more than one dictionary definition is consistent with the use of the word[] in the intrinsic record, the claim term[] may be construed to encompass all such consistent meanings." Id. Any claim interpretation, however, that would exclude a preferred embodiment is "'rarely, if ever, correct.'"

Zimmer, Inc. v. Howmedica Osteonics Corp., No. 03-1428, 2004 U.S. App. LEXIS 10598, at *11 (Fed. Cir. May 26, 2004) (attached as Exhibit C10) (quoting Vitronics, 90 F.3d at 1583).

The Court also has the discretion to admit and rely on prior art proffered by one of the parties, whether or not cited in the specification or the file history, but only when the meaning of the disputed terms cannot be ascertained from a careful reading of the public record. Vitronics, 90 F.3d at 1584. Referring to prior art may make it unnecessary to rely on expert testimony, because prior art may be indicative of what those skilled in the art generally believe a certain term means. Id. Unlike expert testimony, these sources are accessible to the public prior to litigation to aid in determining the scope of an invention. Id.

Finally, "[t]he subjective intent of the inventor when he used a particular term is of little or no probative weight in determining the scope of a claim (except as documented in the prosecution history)." Markman, 52 F.3d at 985. "Rather the focus is on the objective test of what one of ordinary skill in the art at the time of the invention would have understood the term to mean." Id. at 986.

## V. ANALYSIS

### A. Claim 13: Preamble

| Claim Language | Ricoh's Construction | Defendants' Construction[4] |
|---|---|---|
| 13. A computer-aided design process for designing an application specific integrated circuit which will perform a desired function comprising | During manufacture of a desired application specific integrated circuit (ASIC) chip that is designed to perform a specific purpose, a process of designing the desired ASIC using a computer, the process comprising:<br><br>("application specific integrated circuit (ASIC)"= an integrated | A. "A computer-aided design process for designing" -- a process that uses a computer for designing, as distinguished from a computer-aided manufacturing process, which uses a computer to direct and control the manufacturing process.<br><br>B. "application specific integrated circuit" -- an interconnected |

[4] As stated above, for simplification, the ASIC Defendants and Synopsys will be collectively referred to herein as "Defendants."

| Claim Language | Ricoh's Construction | Defendants' Construction[4] |
|---|---|---|
| | circuit chip designed to perform a specific function.) | miniaturized electronic circuit on a single piece of semiconductor material designed to perform a specific function, as distinguished from standard, general purpose integrated circuits, such as microprocessors, memory chips, etc. |

**1. Ricoh's Construction**

This preamble portion of the claim is directed to a process that is part of the manufacture of an "application specific integrated circuit (ASIC)" chip. The term "application specific integrated circuit (ASIC)" should be defined as: "an integrated circuit chip designed to perform a specific function." Ricoh's definition is consistent with the definition of "ASIC" expressly provided in the '432 patent specification:

> An application specific integrated circuit (ASIC) is an integrated circuit chip designed to perform a specific function, as distinguished from standard, general purpose integrated circuit chips, such as microprocessors, memory chips, etc.

'432 patent at 1:13-17.[5] Ricoh's proffered definition is consistent with the ordinary meaning of the term. Any presumption that the term should be given a different "ordinary" meaning is overcome by the explicit definition of the term as provided in the '432 patent specification. Tex. Digital Sys., 308 F.3d at 1204 ("Indeed, the intrinsic record may show that the specification uses the words in a manner clearly inconsistent with the ordinary meaning reflected, for example, in a dictionary definition. In such a case, the inconsistent dictionary definition must be rejected.").

This claim is directed to a process that is used as part of an overall process of manufacturing ASIC chips. As explained in the '432 patent specification, "the present invention, for the first time, opens the possibility for the design and production of ASICs by designers,

[5] All text of the '432 patent, as quoted herein, includes the corrections listed in the Certificate of Correction issued January 14, 1992 (RCL002951-54).

engineers and technicians who may not possess the specialized expert knowledge of a highly skilled VLSI design engineer." '432 patent at 2:15-20 (emphasis added).[6] From the patentee's own Summary of the Invention, it is clear that the inventive "design process" is part of the manufacture of ASIC chips.

Along with the ordinary meaning, the term "computer-aided design," as one would expect from the words themselves, should be defined as: "[t]he use of computers to aid in design layout and analysis" (from the IEEE Standard Dictionary of Electrical and Electronics Terms, Fourth Edition 180 (1988) (RCL011382-88 at RCL011384) (attached as Exhibit No. 3). Consequently, the proper definition of this preamble of the claim in light of the '432 patent specification, together with the ordinary meaning of the claim term, as discussed above, should be interpreted as: "During manufacture of a desired application specific integrated circuit (ASIC) chip that is designed to perform a specific purpose, a process of designing the desired ASIC using a computer . . . ."

For at least these reasons, Ricoh's proposed construction should be adopted.

**2. Defendants' Construction**

Defendants focus their proposed construction of the preamble, as set forth in Exhibit A of the JCC Statement, on the terms "computer-aided design process" and "ASIC." As the first of many of the same assailments on the doctrine of claim construction, Defendants' proposed

[6] Other portions of the '432 patent specification support this proposition. See, e.g., '432 patent Abstract ("The present invention provides a computer-aided design system and method for designing an application specific integrated circuit which enables a user to define architecture independent functional specifications for the integrated circuit and which translates the architecture independent functional specifications into the detailed information needed for directly producing the integrated circuit."); 5:13-46 ("The KBSC system employs a hierarchal cell selection ASIC design approach, . . . . Referring again to FIG. 3, the cells selected . . . are all utilized by the PSCS program 30 to generate the netlist 15. . . . The netlist provides all the necessary information required to produce the integrated circuit. Computer-aided design systems for cell placement and routing are commercially available which will receive netlist data as input and will lay out the respective cells in the chip, generate the necessary routing, and produce mask data which can be directly used by a chip foundry in the fabrication of integrated circuits.").

construction attempts to introduce limitations into the construction of these terms without basis from any of the three intrinsic sources (i.e., claims, specification, and prosecution history) of the public record.

**a. "computer-aided design process"**

Defendants' construction of "computer-aided design process," for example, seeks to add a limitation distinguishing the claim "from a computer-aided manufacturing process, which uses a computer to direct and control the manufacturing process."[7] Beyond the determinative fact that nothing in the public record is cited[8]– or can be found – that provides a basis for imposing such a limitation on the claim, Defendants' proposed limitation hardly proves its point (i.e., a "design" process is distinguished from a "manufacturing" process). Even if there was any evidence that skilled artisans in the field may use the term "computer-aided manufacturing" to refer to the use of a "computer to direct and control the manufacturing process," this would not suggest that a "computer-aided design" process is excluded from the claimed manufacturing process as argued by Defendants. Nothing in the public record indicates intent by the patentee (or any other estoppel operative) to exclude from the scope of the claims the overall manufacturing process. To the contrary, the patentee's "Summary" section of the '432 patent clearly shows that the patentee contemplated the role of its invention in the manufacturing process (i.e., design and production of chips): "the present invention, for the first time, opens the possibility for the design and production of ASICs by designers, engineers and technicians who may not possess the specialized expert knowledge of a highly skilled VLSI design engineer." '432 patent at 2:15-20 (emphasis added).

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[7] JCC Statement, Exhibit A, at 1 (clause "A").

[8] Defendants chiefly rely on extrinsic evidence to support their position and as intrinsic evidence cite only to column 1, lines 9-12 of the '432 patent. JCC Statement, Exhibit A, at 1. This citation, however, must be viewed in light of other parts of the '432 specification that disclose the design and production of ASICS. See Section V.A.1, supra pp. 10-11.

**b. "ASIC"**

With respect to Defendants' proposed construction of the term "ASIC," the parties appear to be largely in agreement,[9] except for the proposed language that would otherwise limit the claim term "ASIC" to "an interconnected miniaturized electronic circuit on a single piece of semiconductor material."[10] This language does not appear in the public record of the '432 patent, nor do Defendants cite any dictionary or treatise in the JCC Statement as the possible source.[11] There is no reason to further limit the ordinary meaning of the term "ASIC" beyond that provided in the '432 patent (as discussed above); therefore, Ricoh's proposal for the definition of the term "ASIC" should be adopted by the Court.

For at least the reasons given above, Defendants' proposed construction of the preamble is improper and Ricoh's proposed construction should be adopted.

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[9] Ricoh does not oppose Defendants' incorporation of the phrase "as distinguished from standard, general purpose integrated circuits, such as microprocessors, memory chips, etc." JCC Statement, Exhibit A, at 2 (clause "B"). Such language is not necessary, however, as the exclusion should be understood or otherwise implicit in Ricoh's definitional language: "designed to perform a specific function." General purpose circuits are, by definition, not designed to perform a "specific" function, but are designed to have general or wide-ranging applicability.

[10] JCC Statement, Exhibit A, at 2 (clause "B").

[11] This is another example of Defendants' reliance on extrinsic evidence, particularly the Declaration of Kowalski. As noted above, see Section II, supra p. 2, the Court specifically prohibited such reliance in these proceedings. Furthermore, the Court need not consider such extrinsic evidence because the public record in this case is unambiguous with respect to this claim language (as is true for all of the claim terms and phrases of claims 13-17 of the '432 patent). Vitronics, 90 F.3d at 1583 ("[W]here the public record unambiguously describes the scope of the patented invention, reliance on any extrinsic evidence is improper.").

## B. Claim 13: Element [1]

| Claim Language | Ricoh's Construction | Defendants' Construction |
|---|---|---|
| [1] storing a set of definitions of architecture independent actions and conditions; | Placing in computer memory a library of definitions of the different architecture independent actions and conditions that can be selected for use in the desired ASIC, where the architecture independent actions and conditions do not imply any structure or implementing technology.<br><br>("architecture independent action and condition"= functional or behavioral aspects of a portion of a circuit (or circuit segment) that does not imply any set architecture, structure or implementing technology.) | C.[12] "actions and conditions"-- are the logical steps and decisions that are represented as rectangles and diamonds in the flowchart; collectively logical operations.<br><br>D. "architecture independent" -- not including (i.e., excluding) a register transfer level (RTL) description or any other description that is hardware architecture dependent. An RTL description consists of: 1) defining the inputs, outputs, and any registers of the proposed ASIC; and, 2) describing for a single clock cycle of the ASIC how the ASIC outputs and any registers are set according to the values of the ASIC inputs and the previous values of the registers; an RTL description defines any control needed for the ASIC.<br><br>E. "a set of definitions of architecture independent actions and conditions" -- a set of named descriptions defining the functionality and arguments for the available logical steps and decisions that may be specified in the flowchart; and excluding a register transfer level description. |

### 1. Ricoh's Construction

This claim element [1] is directed to an action of placing in computer memory a library of definitions. The phrase "architecture independent action and condition" is defined as:

[12] Defendants disagree with Ricoh's definition of "storing" (i.e., "placing in computer memory") for claim 13, element 1 (as well as elements 2 and 3). JCC Statement, Exhibit A, at 3 n.3. Defendants define "storing" as "[s]toring means placing on any storage device 'that is accessible by the processor for the computer system.'" See Section V.B.2.d, infra pp. 22-23.

"functional or behavioral aspects of a portion of a circuit (or circuit segment) that does not imply any set architecture, structure or implementing technology." Ricoh's definition can be ascertained from (and is supported by) the '432 patent. The '432 patent explains that users of the inventive process are able "to define the functional requirements for a desired target integrated circuit." '432 patent at 2:6-14. These requirements may be specified, in accordance with the invention, at an architecture independent functional level that is "easily understood." Id. This level of specification, the '432 patent further explains, "can be defined in a suitable manner, such as in list form or preferably in a flowchart format." Id. at 2:21-24; see also id. at claim 2 ("2. The system as defined in claim 1 wherein said input specification means comprises means for receiving user input of a list defining the series of actions and conditions.").

Fig. 1a of the '432 patent, for example, illustrates an embodiment that utilizes a flowchart representation.[13] This exemplary representation is described in the '432 patent at 3:50-55 ("FIG. 1a shows a functional (or behavioral) architecture independent representation in the form of a flowchart."). As illustrated and described, the representation describes the intended functions or behavior of at least a portion of the ASIC to be produced without reference to (or implication of) any structure to be used in the ASIC.

To the extent it is proper to dissect the phrase "architecture independent actions and conditions" into individual word components,[14] then even under such an analysis, Ricoh's proposed definition is consistent with the ordinary meaning of the claim phrase. As reflected in Merriam-Webster's Ninth New Collegiate Dictionary (1987) (RCL011389-407) (attached as

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[13] As discussed in more detail below, see, e.g., Section V.B.2.a, infra pp. 17-18); Section V.E.1, infra pp. 32-33, claims 13-17 are not limited to a "flowchart representation." The claims broadly read on (and the '432 patent supports) the use of both textual (e.g., list form) and graphical (e.g., flowchart) input descriptions.

[14] Defendants' proposed construction is also improper because it attempts to interpret the individual terms "actions and conditions" and "architecture independent" in isolation, whereas the patentee specifically used the terms together as a single phrase "architecture independent actions and conditions."

Exhibit No. 4), the individual claim terms can be defined as follows: "architecture": "a unifying or coherent form or structure" (101, at RCL011393); "independent": "not dependent[;] . . . not requiring or relying on something else" (612, at RCL011394); "action": "a thing done" (54, at RCL011391); and "condition": "something essential to the appearance or occurrence of something else" (273, at RCL011405A).

Based on the definition of the term as ascertained from the '432 patent itself, as well as the ordinary meaning of the individual terms, the phrase "architecture independent action and condition" is properly defined as "functional or behavioral aspects of a portion of a circuit (or circuit segment) that does not imply any set architecture, structure or implementing technology."

Using the proper definition of "architecture independent action and condition," the claim element [1] should be defined as: "Placing in computer memory a library of definitions of the different architecture independent actions and conditions that can be selected for use in the desired ASIC, where the architecture independent actions and conditions do not imply any structure or implementing technology."

This definition of claim element [1] is supported by the '432 patent specification. In the context of an exemplary embodiment, the '432 patent specification describes the set of definitions (called "macros" for the illustrated embodiment) in a library 23 (Figs. 3 and 4). These definitions are used to "defin[e] various actions which can be specified in the flowchart." '432 patent at 5:20-22. For that embodiment, the '432 patent shows exemplary definitions at Table 1 (id. at 7:29-49). Each of the listed examples of definitions (e.g., "ADD (A, B, C)") has a corresponding description of an architecture independent action or condition (e.g., "C = A + B") that can be performed by the ASIC to be produced. In order to read on at least this embodiment of the invention, this claim element [1] must be construed as noted above. Zimmer, 2004 U.S. App. LEXIS 10598, at *11 (A claim construction that would exclude a preferred embodiment disclosed in the specification is "'rarely, if ever, correct.'" (quoting Vitronics, 90 F.3d at 1583)).

Thus, the proper construction of claim element [1], as consistent with the '432 patent specification and the ordinary meaning of the claim terms, should be as Ricoh has set out above.

### 2. Defendants' Construction

Defendants propose a forced construction that imposes on the claim specific details of one preferred embodiment disclosed in the '432 patent and argues the existence of sweeping estoppels allegedly made during the prosecution history of the '432 patent.

#### a. "actions and conditions"

Defendants' proposed construction, for example, seeks to limit the term "actions and conditions" to "the logical steps and decisions that are represented as rectangles and diamonds in the flowchart; collectively logical operations."[15] By restricting the claim to use of a "flowchart" input, Defendants are attempting to limit the claim scope to the details described in connection with one of the preferred embodiments of the '432 patent. This interpretation is improper because it would exclude the disclosed preferred embodiment dealing with a "list form" of architecture independent functional specification.[16] As noted above, any interpretation that would exclude a preferred embodiment is "'rarely, if ever, correct.'" Zimmer, 2004 U.S. App. LEXIS 10598, at *11 (quoting Vitronics, 90 F.3d at 1583). However, even if the specification described only one embodiment – which it does not – directed to the flowchart input specification, that embodiment would not limit the scope of the claim term. SRI Int'l v. Matsushita Elec. Corp. of Am., 775 F.2d 1107, 1121 n.14 (Fed. Cir. 1985) (attached as Exhibit C11) ("That a specification describes only one embodiment does not require that each claim be limited to that one embodiment."); see also Tex. Digital Sys., 308 F.3d at 1204.

Moreover, patent claim 11 (originally appearing in the '432 patent application as application claim 18) specifically recites "having boxes representing architecture independent actions" and "diamonds representing architecture independent conditions." Such descriptive language does not appear in patent claim 13. It should be evident that, if the patentee intended to

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[15] JCC Statement, Exhibit A, at 3 (clause "C").

[16] See, e.g., '432 patent at 2:21-24.

limit its use of the term "actions and conditions" to the use of specific geometrical shapes such as "rectangles" or "diamonds," the patentee would have used the same or similar limiting language as used in patent claim 11, or at the very least, added the term "flowchart" to patent claim 13, as patentee had done for patent claim 18.

For at least these reasons, Defendants' proposed construction is improper.

**b. "architecture independent"**

Defendants similarly attempt to impose a sweeping category of technology as a limitation of claim scope based on an alleged disclaimer during the '432 patent prosecution history (RCL000001-265) (attached as Exhibit No. 5). In particular, Defendants propose that the claim term "architecture independent" be defined to exclude a "register transfer level (RTL)"-type description, apparently based on a comment by the patentee made during prosecution. See '432 patent prosecution history, Amendment dated April 20, 1989 (Paper No. 6) at 9 (Ex. 5, RCL000207-23 at RCL000215). Defendants appear to define an "RTL"-type description based on characteristics described in U.S. Patent No. 4,703,435 (Darringer et al.) (RCL008592-607) (attached as Exhibit No. 6).[17]

At the outset, Ricoh notes that Defendants are attempting to build into these claim construction proceedings technical arguments that are nothing more than non-infringement arguments having no bearing on the construction of the claim terms. Whether or not an "architecture independent action and condition," for example, covers an RTL-type input

[17] Darringer et al. specifically states: "As pointed out above, the process of this invention begins at step 100 with a register-transfer level description e.g. of the type shown in FIG. 4. The description consists of two parts: a specification of the inputs, outputs and latches of the chip to be synthesized; and a flowchart-like specification of control, describing for a single clock cycle of the machine how the chip outputs and latches are set according to the values of the chip inputs and previous values of the latches. At step 102 in FIG. 2, the register-transfer level description undergoes a simple translation to an initial implementation of AND/OR logic. This AND/OR level is produced by merely replacing specification language constructs with their equivalent AND/OR implementations in a well known manner." Id. at 5:27-41.

description is more about the application of a claim term to an accused device (i.e., the determination of infringement) than it is about the interpretation of that claim term (i.e., claim construction). For this reason alone, Defendants' proposed construction is improper.[18] SRI Int'l, 775 F.2d at 1118 ("A claim is construed in the light of the claim language, the other claims, the prior art, the prosecution history, and the specification, *not* in light of the accused device. Contrary to what MEI's counsel wrote the district court, claims are not construed 'to cover' or 'not to cover' the accused device. That procedure would make infringement a matter of judicial whim. It is only *after* the claims have been *construed without reference to the accused device* that the claims, as so construed, are applied to the accused device to determine infringement.").[19]

Moreover, accepting the definition proposed by Defendants would exclude one of the exemplary implementations of the patented invention, as explicitly disclosed in the '432 patent. The '432 patent, for example, discloses a specific implementation of an architecture independent functional specification in Fig. 10 of the '432 patent. This exemplary specification can easily be characterized as a description that falls within the category of descriptions excluded by Defendants' proposed construction (i.e., a "description [that] consists of: 1) defining the inputs, outputs, and any registers of the proposed ASIC; and, 2) describing for a single clock cycle of the ASIC how the ASIC outputs and any registers are set according to the values of the ASIC inputs and the previous values of the registers").[20] Defendants' construction would thus exclude

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[18] However, if there were a "clear disclaimer" or "clear disavowal" of the scope, then it would be proper.

[19] See also Union Oil Co. v. Atl. Richfield Co., 208 F.3d 989, 995 (Fed. Cir. 2000) (attached as Exhibit C12) ("'In claim construction the words of the claims are construed independent of the accused product, in light of the specification, the prosecution history, and the prior art. . . . [T]he construction of claims is simply a way of elaborating the normally terse claim language[ ] in order to understand and explain, but not to change, the scope of the claims.'" (quoting Scripps Clinic & Research Found. v. Genentech, Inc., 927 F.2d 1565, 1580 (Fed. Cir. 1991) (attached as Exhibit C13)) (emphasis added) (alterations in original).

[20] JCC Statement, Exhibit A, at 4 (clause "D").

a preferred embodiment of the '432 patent. Such a construction is "'rarely, if ever, correct.'" Zimmer, 2004 U.S. App. LEXIS 10598, at *11 (quoting Vitronics, 90 F.3d at 1583).

Nevertheless, to the extent the Court deems it appropriate, Ricoh submits the following comments. During prosecution of the '432 patent, the patentee distinguished the invention over Darringer et al., asserting that the prior art used an input in the form of a register transfer language (RTL)-level flowchart. The patentee explained: "In order for a designer to utilize the Darringer system, he/she must possess a sophisticated understanding of the complexities of the circuit logic itself and therefore have the specialized expert knowledge of a highly skilled VLSI design engineer." Amendment dated April 20, 1989 (Paper No. 6) at 9 (Ex. 5, RCL000215).

The present invention as defined by process claim 13 involves providing a functional, structurally independent input description. In contrast, Darringer et al. discloses using a structurally dependent RTL-level input to describe the behavior of the chip that is to be designed. The "RTL-level" used in Darringer et al. (as well as other prior art references cited in the '432 patent prosecution history) requires the input of a "basic" or "primitive Boolean"-type specification of register inputs, outputs, and timing between registers during a single clock cycle of the chip operation. See, e.g., Darringer et al. at 5:27-35. Darringer et al. states that this type of RTL-level input is simply translated (in well-known manner) into an initial implementation of AND/OR logic by replacing input RTL constructs with their equivalent AND/OR implementations. Id. at 5:35-47.

The requirement of specifying the individual inputs, outputs, and registers for a single clock cycle, together with the fact that the specification can be so easily (and directly) translated into AND/OR logic, indicates that the RTL-level input is a more basic "structural" input. Although it can be used to describe the functional aspects of a desired chip, it does not do so in a purely higher level functional manner that allows higher level concepts such as addition, multiplication, etc. (or other manner that is free of basic Boolean specifications). The

"structural" RTL-type description utilized in Darringer et al. therefore is not "architecture independent."

Ricoh notes that VHDL and Verilog are hardware description languages ("HDLs") used in the field of the invention that have been referred to as "RTL-type" languages. These HDLs, however, allow a designer to describe desired operations or functionality of a proposed design without regard to structural details (such as required by Darringer et al.). Representation exclusively in Boolean terms is thus not required. This type of "RTL-level" is considered to be "functional RTL" as contrasted to the "basic" or "primitive RTL" of Darringer et al.

For any estoppel attributed to the patentee's arguments distinguishing the claimed invention over an "RTL"-type input description, it should be made clear that the patentee used the term "RTL" in referring to Darringer et al. (and other prior art systems) that had "basic" or "primitive RTL" type of inputs, which were not covered by the '432 patent claims. The patentee did not disclaim coverage, however, of systems that used "functional RTL" type of inputs (e.g., VHDL/Verilog-based systems) that were architecture independent. Thus, to the extent it is necessary to clarify what is excluded from the proper interpretation of the term "architecture independent actions and conditions," the exclusion should be limited to "basic" or "primitive RTL-type descriptions" and not the entire category of "RTL" descriptions, as contended by Defendants. The patentee is presumed to have the full scope of coverage afforded the ordinary meaning of the claim terms unless "the inventor has disavowed or disclaimed scope of coverage, by using words or expressions of manifest exclusion or restriction, representing a clear disavowal of claim scope." Tex. Digital Sys., 308 F.3d at 1204. No such "manifest exclusion" or "clear disavowal" of the scope proposed by Defendants is present here. At best, any disclaimer is far from the "clear and unmistakable" disavowal needed to limit the scope of the claim. Sunrace, 336 F.3d at 1306 ("To be given effect, such a disclaimer must be 'clear and unmistakable.'" (quoting Omega, 334 F.3d at 1325)). Indeed, "[b]ecause the statements in the prosecution history are subject to multiple reasonable interpretations, they do not constitute a clear and unmistakable departure from the ordinary meaning of the [claim term at issue]." Golight, 355 F.3d at 1332.

**c. "a set of definitions of architecture independent actions and conditions"**

Taking into account their definitions of "actions and conditions" and "architecture independent," Defendants define claim element [1] to be: "a set of named descriptions defining the functionality and arguments for the available logical steps and decisions that may be specified in the flowchart; and excluding a register transfer level description."[21] In addition to the incorporation of improper definitions of the terms "actions and conditions" and "architecture independent," as discussed above, the proposed interpretation of this claim element is improper because it attempts to limit the scope of the claim element to one of the preferred embodiments disclosed in the '432 patent.

Ricoh cannot be certain, but Defendants' use of the terms "named descriptions" and "arguments" appears to be intended by Defendants to encompass the "macros" shown in Table 1 of the '432 patent (at 7:29-49) and described at 7:24-28. While Defendants' description may (arguably) be accurate in describing the preferred embodiment disclosed in the '432 patent, nothing in the description or anything else in the '432 patent claims, specification, or prosecution history compels the conclusion that the preferred embodiment is the outer limit on the scope of claim element [1]. SRI Int'l, 775 F.2d at 1121 n.14 ("That a specification describes only one embodiment does not require that each claim be limited to that one embodiment."); see also Tex. Digital Sys., 308 F.3d at 1204.

For this reason alone, Defendants' proposed construction is improper and should not be adopted.

**d. "storing"**

Although no contrary construction was formally proposed, Defendants appear to "disagree with Ricoh's definition of 'storing' on this [claim] step." JCC Statement, Exhibit A, at

[21] JCC Statement, Exhibit A, at 5 (clause "E").

3 n.3. Defendants state: "Storing means placing on any storage device 'that is accessible by the processor for the computer system.' IBM Dictionary of Computing at 654 (Attachment 16, DEF083932-DEF084703)." Id. (This quoted language provided by Defendants, however, appears nowhere at page 654 of the IBM Dictionary of Computing.) It is not clear where any controversy exists in this regard, as each of the dictionary entries for the term "storing" as they appear in the cited IBM Dictionary of Computing at 654 (DEF084598) (attached as Exhibit No. 7) is consistent with Ricoh's proposed definition of "placing in computer memory": "storing (1) The action of placing data into a storage device. (2) To place data into a storage device. (3) To retain data in a storage device." A similar definition is provided in Merriam-Webster's Ninth New Collegiate Dictionary 1162 (1987): "store": "to place or leave in a location (as a warehouse, library, or computer memory) for preservation or later use or disposal" (RCL011411-13 at RCL011413) (attached as Exhibit No. 8) (emphasis added).

As the only evidence cited by Defendants against Ricoh's proposed language is consistent with Ricoh's proposed construction, Ricoh's definition of "storing" (i.e., placing in computer memory) should be adopted for claim element [1], as well as for claims elements [2] and [3].

For at least the reasons given above, Defendants' proposed construction of claim element [1] is improper and Ricoh's proposed construction should be adopted.

### C. Claim 13: Element [2]

| Claim Language | Ricoh's Construction | Defendants' Construction |
|---|---|---|
| [2] storing data describing a set of available integrated circuit hardware cells for performing the actions and conditions defined in the stored set; | Placing in computer memory a library of cell information that describe hardware cells capable of performing the different architecture independent actions and conditions placed in the library of definitions.<br>("hardware cells"= previously designed circuit components or structure that have specific | F. "hardware cells" -- logic blocks for which the functional level (e.g., register transfer level), logic level (e.g., flip flop and gate level), circuit level (e.g., transistor level), and layout level (e.g., geometrical mask level) descriptions are all defined.<br>G. "data describing a set of available integrated circuit |

| Claim Language | Ricoh's Construction | Defendants' Construction |
|---|---|---|
| | physical and functional characteristics used as building blocks for implementing an ASIC to be manufactured.) | hardware cells for performing the actions and conditions defined in the stored set" -- a set of named integrated circuit hardware cells that includes at least one hardware cell for each stored definition that may be specified for the available logical steps and decisions; where each named hardware cell has corresponding descriptions at the functional level (e.g., register transfer level), logic level (e.g., flip-flop and gate level), circuit level (e.g., transistor level), and layout level (e.g., geometrical mask level) that are all defined. |

**1. Ricoh's Construction**

This claim element [2] is directed to a process of placing in computer memory a library of cell information. As a preliminary matter, it is noted that the term "hardware cells" is defined as: "previously designed circuit components or structure that have specific physical and functional characteristics used as building blocks for implementing an ASIC to be manufactured." As described in the '432 patent, the "hardware cells" are "needed to achieve the functional specifications [of the ASIC to be produced]." '432 patent at 2:34-36.

As claimed, data describing the available "hardware cells" is stored. In this regard, the '432 patent specifies that the "hardware cells" are "selected from a cell library of previously designed hardware cells of various functions and technical specifications." '432 patent at 2:36-39. These hardware cells are included in "an architecture specific structural level definition of an integrated circuit, which can be used directly to produce the ASIC." Id. at 2:27-34. In explaining the utility of the "hardware cells" and the storage of the cells in a "cell library," the '432 patent states:

> The KBSC system employs a hierarchal cell selection ASIC design approach, as is illustrated in FIG. 4. Rather than generating every required hardware cell from scratch, the system draws upon a cell library 34 of previously designed, tested and proven hardware cells of various types and

> of various functional capabilities with a given type. . . . For each macro function in the macro library 23 there may be several hardware cells in the cell library 34 of differing geometry and characteristics capable of performing the specified function.

Id. at 5:14-25.

From a plain reading of the claim language in light of these teachings of the '432 patent, it is apparent that the proper interpretation of claim element [2] should be: "Placing in computer memory a library of cell information that describe hardware cells capable of performing the different architecture independent actions and conditions placed in the library of definitions," where the term "hardware cells" should be defined as "previously designed circuit components or structure that have specific physical and functional characteristics used as building blocks for implementing an ASIC to be manufactured."

For at least these reasons, Ricoh's proposed construction should be adopted.

**2. Defendants' Construction**[22]

As with the previous claim element [1], Defendants attempt to improperly impose on claim element [2] specific details from a preferred embodiment disclosed in the '432 patent. Defendants, for example, include in their proposed definition of the term "hardware cells" all of the different types of information described in the '432 patent as being stored for the cells of cell library 34. '432 patent at 9:24-34. Nowhere in this description (or any other portion of the '432 patent, nor in its prosecution history) is there any indication that these four types of information must be included in the cell library recited in claim 13 of the '432 patent. To the extent the preferred embodiment imposes any requirement at all, it is that the cell library contains "previously designed hardware cells of various functions and technical specifications." Id. at 2:36-39. As noted previously, "[t]hat a specification describes only one embodiment does not require that each claim be limited to that one embodiment." SRI Int'l, 775 F.2d at 1121 n.14; see

[22] To the extent applicable, Ricoh incorporates its arguments previously set forth above with respect to Defendants' proposed definition of "storing." See Section V.B.2.d, supra pp. 22-23.

also Tex. Digital Sys., 308 F.3d at 1204. Defendants' proposed construction should not be adopted for this reason alone.

Defendants go further, however, in attempting to narrowly construe claim element [2] to be: "a set of named integrated circuit hardware cells that includes at least one hardware cell for each stored definition that may be specified for the available logical steps and decisions, . . . ."[23] First, Defendants introduce the limitation that the hardware cells are "named" cells. This limitation appears to be directed to one of the exemplary attributes listed in the '432 patent for the preferred embodiment. See '432 patent at 9:35-51 (including the "cell name" attribute at 9:36). As with the definition of "hardware cells," nothing in the '432 patent itself nor in its prosecution history compels a finding that the "cell name" is a required feature of any embodiment of claim element [2].

Second, Defendants introduce a requirement of the claim that there is "at least one hardware cell for each stored definition." This attempt to restrict the claims is even more specious because there is no disclosure whatsoever in the '432 patent that supports this requirement of the cell library. As the claim language, the specification, and even the prosecution history are completely devoid of any requirement that there is "at least one hardware cell for each stored definition," Defendants' proposed construction should not be adopted on this basis alone.

For at least the reasons given above, Defendants' proposed construction of claim element [2] is improper and Ricoh's proposed construction should be adopted.

### D. Claim 13: Element [3]

| Claim Language | Ricoh's Construction | Defendants' Construction |
|---|---|---|
| [3] storing in an expert system knowledge base a set of rules for | Placing in an expert system knowledge base, that uses a | H. "expert system" -- software executing on a computer system |

[23] JCC Statement, Exhibit A, at 6 (clause "G") (emphasis added).

| Claim Language | Ricoh's Construction | Defendants' Construction |
|---|---|---|
| selecting hardware cells to perform the actions and conditions; | computer memory, a plurality of rules for selecting among the hardware cells placed in the hardware cell library, wherein the rules comprise the expert knowledge of highly skilled VLSI designers formulated as prescribed procedures.<br><br>("expert system knowledge base"= database used to store expert knowledge of highly skilled VLSI designers.)<br><br>("rules"= the expert knowledge of highly skilled VLSI designers formulated as prescribed procedures.) | that attempts to embody the knowledge of a human expert in a particular field and then uses that knowledge to simulate the reasoning of such an expert to solve problems in that field. This system is comprised of a knowledge base containing rules, working memory containing the problem description, and an inference engine. It solves problems through the selective application of the rules in the knowledge base to the problem description, as distinguished from conventional software, which uses a predefined step-by-step procedure (algorithm) to solve problems.<br><br>I. "Knowledge base" -- the portion of the expert system containing a set of rules embodying the expert knowledge for the particular field.<br><br>J. "a set of rules for selecting hardware cells to perform the actions and conditions" -- a set of rules, each having an antecedent portion (IF) and a consequent portion (THEN), embodying the knowledge of expert designers for application specific integrated circuits, which enables the expert system to map the specified stored definitions for each logical step and decision represented in the flowchart to a corresponding stored hardware cell description. |

**1. Ricoh's Construction**

This claim element is directed to a process step of placing in a database rules for selecting hardware cells. As part of the definition, the term "expert system knowledge base" refers to a "database used to store expert knowledge of highly skilled VLSI designers." This definition is derived from the express teachings of the '432 patent. The '432 patent

specification, for example, describes an expert system knowledge base used in an exemplary embodiment:

> The knowledge base 35 contains ASIC design expert knowledge required for data path synthesis and cell selection. . . .
>
> . . . . Using a rule based expert system with a knowledge base 35 extracted from expert ASIC designers, the KBSC system selects from the cell library 34 the optimum cell for carrying out the desired function.

'432 patent at 5:6-29. The illustrated "knowledge base" contains information in the form of rules. See, e.g., id. at 8:65-9:5 ("The knowledge base of Cell Selector 32 contains information (rules) . . . . The above information is stored in the knowledge base 35 as rules."). In the '432 patent, "[t]he rules are stored in a database." Id. at 11:30-32.

It is apparent from these passages that an "expert system knowledge base" is a collection of data that represents knowledge obtained from experts in ASIC design. Such a collection of data must be maintained in a "database used to store expert knowledge of highly skilled VLSI designers."

Furthermore, as part of the interpretation of this claim element, the term "rules" should be defined as: "the expert knowledge of highly skilled VLSI designers formulated as prescribed procedures." This definition is derived primarily from the teachings of the '432 patent, as summarized above, in conjunction with the ordinary meaning of the term "rules" (i.e., "a prescribed guide for conduct or action[;] . . . an accepted procedure, custom, or habit," Merriam-Webster's Ninth New Collegiate Dictionary 1030 (1987) (RCL011389-407 at RCL011405) (attached as Exhibit No. 4)).

With the proper definitions of the terms "expert system knowledge base" and "rules," the proper construction of this claim element [3] should be: "Placing in an expert system knowledge base, that uses a computer memory, a plurality of rules for selecting among the hardware cells placed in the hardware cell library, wherein the rules comprise the expert knowledge of highly skilled VLSI designers formulated as prescribed procedures."

For at least these reasons, Ricoh's proposed construction should be adopted.

### 2. Defendants' Construction[24]

Defendants continue their endeavor to carve out non-infringement arguments and theories through crafty definitions of claim terms. Here, Defendants go so far as to rewrite the claim term "expert system knowledge base" into two separate terms: "expert system" and "knowledge base" for interpretation in isolation. Defendants' construction is improper on its face.

#### a. "expert system"

First, a plain, grammatical reading of the claim language shows that claim element [3] clearly recites the term "expert system" as an adjective or other modifier for the noun "knowledge base." As a modifier, the term "expert system" does not impute its own limitations on the overall process claimed, but rather on the "knowledge base" itself. See ZMI Corp. v. Cardiac Resuscitator Corp., 844 F.2d 1576, 1580-81 (Fed. Cir. 1988) (attached as Exhibit C14) (finding that claim term "low current density" that grammatically modified claim term "electrodes" has meaning as a limitation of the claimed electrodes, not as a limitation of the claimed system).

Second, the position of Defendants is also inconsistent with the teachings of the '432 patent. The '432 patent makes it clear that the rules or knowledge of the system is stored in the "knowledge base," not in a system known as an "expert system." See, e.g., '432 patent at 5:6-8 ("The knowledge base 35 contains ASIC design expert knowledge required for data path synthesis and cell selection."); 8:29-30 ("The cell selector uses a knowledge base extracted from VLSI design experts to make the cell selection."); 8:65-66 ("The knowledge base of Cell Selector 32 contains information (rules) relating to: . . . ."); 9:4-5 ("The above information is stored in the knowledge base 35 as rules."). The term "expert system knowledge base" thus is

[24] To the extent applicable, Ricoh incorporates its arguments previously set forth above with respect to the term "storing." See Section V.B.2.d, supra pp. 22-23.

intended to capture the features of a "knowledge base" that may be used in an expert system, but not intended to capture an "expert system" that uses a "knowledge base."

Third, Ricoh's proposed construction is further apparent from the prosecution history, where patent claims 9 and 13 (corresponding to application claims 15 and 20, respectively) were simultaneously amended and subsequently allowed on the next Office Action. Amendment dated November 20, 1989 (Paper No. 9) at 2-5 (Ex. 5, RCL000229-37 at RCL000230-33). Patent claim 9 was amended to explicitly claim "an expert system including a knowledge base containing rules." Id. at 3 (RCL000231). Patent claim 13, however, was amended (at the same time) to merely refer to an "expert system knowledge base." Id. at 4 (RCL000232). If the patentee had intended to encompass both an "expert system" and a "knowledge base" for the process of patent claim 13, the patentee would have used the same language as was added to patent claim 9.

The Court therefore should not construe the term "expert system" as a separate limitation on the overall process of claim 13.

Even if the Court must somehow find that the claim term "expert system knowledge base" requires the presence of both an "expert system" and a "knowledge base," nothing in the claim language, the specification, or the prosecution history mandates that the "expert system" contain specific elements such as a "working memory" or an "inference engine,"[25] as proposed by Defendants.[26] As with the previous claim elements, Defendants are forcing a restriction of the claims to a preferred embodiment of the '432 patent. Such a restriction is improper. SRI Int'l, 775 F.2d at 1121 n.14; see also Tex. Digital Sys., 308 F.3d at 1204. Defendants' proposed construction should not be adopted.

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[25] JCC Statement, Exhibit A, at 7 (clause "H").

[26] Here again, Defendants can only rely on extrinsic evidence (particularly the Declaration of Kowalski) in hopes of imputing these additional limitations in the claim. Moreover, Defendants apparently seek to have these particular requirements included in the Court's interpretation of the term "expert system" solely for the purpose of fashioning some type of non-infringement theory (e.g., based on an alleged lack of an "inference engine") at trial.

**b. "knowledge base"**

To the extent that Defendants' proposed construction is not read to incorporate any requirements or restrictions on the presence of an "expert system" having a "working memory" and an "inference engine," it appears that Defendants' proposed definition of "knowledge base" is substantially consistent with that proposed by Ricoh. There is no significant basis therefore to contest the adoption of Ricoh's proposed construction of the term "expert system knowledge base" to mean: "database used to store expert knowledge of highly skilled VLSI designers."

**c. "a set of rules for selecting hardware cells to perform the actions and conditions"**

Defendants again offer a construction of claim language that is intended to limit the claims to a preferred embodiment of the '432 patent. Defendants, for example, assert that the claimed "rules" must each have the format of "an antecedent portion (IF) and a consequent portion (THEN)."[27] This format was disclosed in the '432 patent in connection with a preferred embodiment of the invention. See, e.g., '432 patent at 11:1-14. Even though this format was the only format specifically disclosed as an embodiment of the claimed "rules," nothing in the public record justifies restriction of the claimed "rules" to the exemplary format disclosed as the preferred embodiment. See SRI Int'l, 775 F.2d at 1121 n.14; Tex. Digital Sys., 308 F.3d at 1204. Defendants' proposed construction should not be adopted for this reason alone.

Defendants then seek to impose the additional requirement: "embodying the knowledge of expert designers for application specific integrated circuits."[28] To the extent that Defendants perceive a distinction between the knowledge of designers for ASICs and the knowledge of designers skilled in VLSI design, this claim should be construed broadly to include either skill level. Such an interpretation is evident from the '432 patent specification, as it

[27] JCC Statement, Exhibit A, at 8-9 (clause "J").

[28] JCC Statement, Exhibit A, at 8-9 (clause "J") (emphasis added).

discloses the knowledge of the system being extracted from both ASIC designers and VLSI designers. See, e.g., '432 patent at 2:58-61 ("The KBSC utilizes a knowledge based expert system, with a knowledge base extracted from expert ASIC designers with a high level of expertise in VLSI design . . . ."); 4:8-11 ("In the KBSC system of the present invention, however, integrated circuits can be designed at a functional level because the expertise in VLSI design is provided and applied by the invention."); 5:6-8 ("The knowledge base 35 contains ASIC design expert knowledge required for data path synthesis and cell selection."); 5:25-29 ("Using a rule based expert system with a knowledge base 35 extracted from expert ASIC designers, the KBSC system selects from the cell library 34 the optimum cell for carrying out the desired function.").

For at least the reasons given above, Defendants' proposed construction of claim element [3] is improper and Ricoh's proposed construction should be adopted.

### E. Claim 13: Element [4]

| Claim Language | Ricoh's Construction | Defendants' Construction |
|---|---|---|
| [4] describing for a proposed application specific integrated circuit a series of architecture independent actions and conditions; | A user describing an input specification containing the desired functions to be performed by the desired ASIC. | K. "describing for a proposed application specific integrated circuit a series of architecture independent actions and conditions" -- the designer represents a sequence of logical steps (rectangles) and decisions (diamonds), and the transitions (lines with arrows) between them in a flowchart format for a proposed application specific integrated circuit. |

#### 1. Ricoh's Construction

This claim element is directed to the input of a description of the desired functions to be performed by the ASIC to be produced. Ricoh incorporates the definitions (and the bases

therefor) as set forth above for the terms "application specific integrated circuit (ASIC)"[29] and "architecture independent actions and conditions."[30] Ricoh notes that the plain and ordinary meaning of the term "describe" is: "1: to represent or give an account of in words <~ a picture> 2: to represent by a figure, model, or picture: DELINEATE." Merriam-Webster's Ninth New Collegiate Dictionary 343 (1987) (RCL011389-407 at RCL011398) (attached as Exhibit No. 4). It is noted, however, that the use of the term "describe" or "describing" has no specialized technical meaning, and thus, there is no reason to assign any specific definition in order to properly construe claim element [4]. In light of the previously construed terms "application specific integrated circuit (ASIC)" and "architecture independent actions and conditions," the proper interpretation of claim element [4] should be: "A user describing an input specification containing the desired functions to be performed by the desired ASIC."

Ricoh's interpretation is consistent with the disclosure in the '432 patent. The '432 patent teaches that the claimed process "enables a user to define the functional requirements for a desired target integrated circuit, using an easily understood architecture independent functional level representation." '432 patent at 2:6-15. As taught in the '432 patent, the format of the input description may be in any suitable form, including textual or graphical:

> The architecture independent functional specifications of the desired ASIC can be defined in a suitable manner, such as in list form or preferably in a flowchart format. The flowchart is a highly effective means of describing a sequence of logical operations, and is well understood by software and hardware designers of varying levels of expertise and training. From the flowchart (or other functional specifications), the system and method of the present invention translates the architecture independent functional specifications into an architecture specific structural level definition of an integrated circuit, which can be used directly to produce the ASIC.

Id. at 2:21-34 (emphasis added).

For at least these reasons, Ricoh's proposed construction should be adopted.

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[29] See Section V.A.1, supra pp. 10-11.

[30] See Section V.B.1, supra pp. 14-16.

**2. Defendants' Construction**

As with each of the previous elements, Defendants assert a claim construction that blatantly restricts claim element [4] to the details of an input device described in the preferred embodiment of the '432 patent. In particular, Defendants' proposed construction attempts to limit the "describing" step to representations using "rectangles," "diamonds," and "lines with arrows" in a "flowchart format."[31] As noted previously, however, examples and embodiments in the specification should not be read to limit the scope of a claim term. Tex. Digital Sys., 308 F.3d at 1204 ("But if the meaning of the words themselves would not have been understood to persons of skill in the art to be limited only to the examples or embodiments described in the specification, reading the words in such a confined way would mandate the wrong result and would violate our proscription of not reading limitations from the specification into the claims."); see also Teleflex, 299 F.3d at 1326 ("limitations from the specification are not to be read into the claims"). Defendants seek to go even further than what the Federal Circuit disallowed, since Defendants propose an interpretation that would limit the claim to just one of the embodiments disclosed in the '432 patent. Defendants' proposed construction should be deemed improper on that basis alone.

Moreover, as noted above,[32] patent claim 11 particularly points out the patentee's invention using "boxes," "diamonds," and "lines with arrows" for use in a "flowchart format." If the patentee intended to limit patent claim 13 to the same scope (i.e., flowchart format), the patentee would have used the same claim language, or at the very least, added the term "flowchart" to patent claim 13, as patentee had done for patent claim 18.

Defendants cited (JCC Statement, Exhibit A, at 11) the Examiner Interview Summary Record (mailed October 19, 1989 (Paper No. 8) (Ex. 5, RCL000228)) that appears in the prosecution history for support of their position. Placed in its proper context, the Summary

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[31] JCC Statement, Exhibit A, at 11 (clause "K").

[32] See Section V.B.2.a, supra pp.17-18.

Record does not serve as a basis for importing implicit limitations into the scope of claim 13 of the '432 patent.

The Summary Record was issued in order to document (from the examiner's perspective) an interview conducted between the attorney prosecuting the '432 patent application and the examiner examining the application. The examiner stated in the Summary Record that application claims 1, 5, 15, 18, 20, and 27 were discussed and indicated an agreement was believed to have been reached as to some or all the claims.

In particular, the examiner agreed that certain features of the '432 patent invention are considered patentable over the prior art discussed at the interview, i.e., U.S. Patent No. 4,703,435 (Darringer et al.). The features identified by the examiner were: "flowchart editor" and "expert system for translating the flowchart into a netlist defining the necessary hardware cells of the integrated circuit." The examiner further stated: "Thus, applicant's attorney will amend the claims to include these features."

The Summary Record proves nothing more than that the examiner believed that the outstanding rejection of the then-pending application claims could be overcome if the enumerated features were added to the rejected application claims. Apparently, it was the examiner's perception that the rejected claims would be amended to include the enumerated features. There is no statement or other indication, however, that the examiner deemed such an amendment to be the only way to overcome the rejection of the application claims. Nor is there any indication in the Summary Record (or the prosecution history as a whole) that the patentee's attorney considered the examiner's statement a requirement that must be followed if the patentee was to obtain a patent on application claims 1, 5, 15, 18, 20, and 27. This conclusion is readily apparent from the fact that patent application claim 20, which became patent claim 13, was not amended to add such features.

The Summary Record thus cannot be deemed an agreement between the examiner and the patentee (through its attorney) to incorporate the enumerated features into all of the then-pending claims. Instead, it must be viewed for what it is – simply an indication that the examiner

would need no further discussion or persuasion to remove the rejection of any claim that was amended to incorporate at least those features.

Ricoh's proposed construction is consistent with the events that occurred subsequent to the issuance of the Summary Record. In the Amendment dated November 20, 1989 (Paper No. 9) (Ex. 5, RCL000229-37), for example, the patentee did not amend any of the claims to incorporate all of the enumerated features. Indeed, the patentee canceled application claim 1. With respect to claims 5, 15, 20, and 27, the patentee amended the claims to incorporate certain features previously recited in dependent claims, and provided arguments why the amended claims should be considered patentable over the prior art.

If the Summary Record was intended to be a binding agreement, the patentee would have merely added the enumerated features to ensure allowance (or at least withdrawal of the rejection) of claim 1. Moreover, the patentee would have made essentially the same amendments to application claims 5, 15, 20, and 27 and never attempted to distinguish the claims over the prior art. The patentee, for example, could have simply stated that the amended claims included the features discussed during the interview, and thus, as (allegedly) agreed in the interview, are patentable over the prior art. Indeed, the patentee had done just that for claim 18; the patentee merely referred to the substance of the interview and provided no substantive discussion.

In contradistinction, with application claims 5, 15, 20, and 27, the patentee chose to explore the varied scope of claims that could be obtained beyond the mere coverage afforded by the enumerated features. By varying the scope of amendments to these claims and arguing the distinctive points individually, the patentee sought (and obtained) a varying degree of protection beyond that originally proposed by the examiner during the interview (which was represented by application claim 18). The patentee was not limited by the characterization of the claimed subject matter provided by the examiner in the Summary Record. Eastman Kodak Co. v. Goodyear Tire & Rubber Co., 114 F.3d 1547, 1556 (Fed. Cir. 1997),[33] (attached as Exhibit C15)

[33] In Eastman Kodak, the court stated the following. "During the 1993 reexamination, the

abrogated on other grounds by Cybor Corp. v. FAS Techs., Inc., 138 F.3d 1448 (Fed. Cir. 1998) (en banc) (attached as Exhibit C16). It would thus be improper to read into patent claim 13 any of the features stated in the Examiner Interview Summary Record.

For at least the reasons given above, Defendants' proposed construction of claim element [4] is improper and Ricoh's proposed construction should be adopted.

### F. Claim 13: Element [5]

| Claim Language | Ricoh's Construction | Defendants' Construction |
|---|---|---|
| [5] specifying for each described action and condition of the series one of said stored definitions which corresponds to the desired action or condition to be performed; and | Specifying for each desired function to be performed by the desired ASIC one of the definitions of the architecture independent actions and conditions stored in the library of definitions that is associated with the desired function.<br><br>("specifying"= mapping or associating a desired function to be performed by the manufactured ASIC with a definition from the library of definitions.) | L. "specifying for each described action and condition of the series one of said stored definitions" -- the designer assigns one definition from the set of stored definitions for each of the described logical steps and decisions represented in the flowchart.<br><br>M. "which corresponds to the desired action or condition to be performed" -- each specified definition must correspond to the intended step or decision to be performed. |

#### 1. Ricoh's Construction

This claim element is directed to the mapping or associating of one of the definitions of architecture independent actions and conditions defined in the "storing a set of definitions"

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examiner's Reexamination Interview Summary Form stated that this claim language meant 'not exceeding the initial crystallization temperature during further crystallization and after condensation.' To the extent that the examiner's certificate purports to ascribe meaning not found in the claim language, this court must not permit prosecution history evidence to 'enlarge, diminish, or vary' the meaning of claim language. The claim language does not mention 'initial crystallization' as distinct from 'further crystallization.' Nor did the 1993 reexamination require any changes in claim language." Id. (quoting Markman, 52 F.3d at 980).

step (claim element [1]) to an input function described in the claimed "describing" step (claim element [4]). Ricoh incorporates the definition (and the bases therefor) for the term "architecture independent actions and conditions," as set forth above.[34] As part of the proper interpretation of this claim element [5], the term "specifying," to be consistent with the teachings of the '432 patent, should be defined as: "mapping or associating a desired function to be performed by the manufactured ASIC with a definition from the library of definitions."

The '432 patent, for example, describes that the invention performs the acts of selecting optimum hardware cells based on functional descriptions "as specified by the macros assigned to each action." '432 patent at 8:23-26 (emphasis added).[35] In the exemplary embodiment, the macros may be "mapped" to actions manually through user commands. Id. at 7:24-25 ("Edit actions allows the designer to assign actions to each box."). The macros also may be "mapped" automatically through application of rules. Id. at 9:14-18 ("Rules of the following type are applied during this stage. . . . map actions to macros." (emphasis added)); see also id. at 13:5-7 ("The macro instruction associated with state21 moves the value in the register sum to cv." (emphasis added)); 13:28-31 ("The macros associated with the states shown in FIG. 10 correspond to those defined in Table 1 above and define the particular actions which are to be performed at the respective states." (emphasis added)).

In order to be consistent with the teachings of the invention, including the description of the preferred embodiments in the '432 patent, the claim element [5] should be defined as: "Specifying for each desired function to be performed by the desired ASIC one of the definitions of the architecture independent actions and conditions stored in the library of definitions that is associated with the desired function," where the term "specifying" should be defined as

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[34] See Section V.B.1, supra pp. 14-16.

[35] As noted above, see Section V.B.1, supra pp. 16, the term "macros" is used in the '432 patent in its description of an embodiment of the claimed "definitions of architecture independent actions and conditions."

"mapping or associating a desired function to be performed by the manufactured ASIC with a definition from the library of definitions."

For at least these reasons, Ricoh's proposed construction should be adopted.

**2. Defendants' Construction**

Consistent with their overall strategy of seeking to read additional detailed limitations into the claims, Defendants seek to construe this claim element [5] so that it is limited to a manual operation performed by the user. JCC Statement, Exhibit A, at 13 (clause "L") ("'specifying for each described action and condition . . .'– the designer assigns one definition from the set . . ."). Defendants thus hope to limit the construction to detailed aspects of a specific embodiment disclosed in the '432 patent in which a user assigns macros to each box of an input flowchart. See '432 patent at 7:24-26.

Defendants' proposed construction is improper because it ignores the basic rules of claim construction. First, as noted previously, limiting the construction of a claim to a preferred embodiment merely because it is the only embodiment disclosed, as attempted by Defendants, is improper. SRI Int'l, 775 F.2d at 1121 n.14 ("That a specification describes only one embodiment does not require that each claim be limited to that one embodiment."); see also Tex. Digital Sys., 308 F.3d at 1204. Second, Defendants' construction is particularly improper here because it would exclude a preferred embodiment disclosed in the specification in which the assignment of the macros is done automatically.[36] Such a construction is "'rarely, if ever, correct.'" Zimmer, 2004 U.S. App. LEXIS 10598, at *11 (quoting Vitronics, 90 F.3d at 1583).

For at least the reasons given above, Defendants' proposed construction of claim element [5] is improper and Ricoh's proposed construction should be adopted.

[36] As noted above, see Section V.F.1, supra p. 38, the '432 patent discloses both a manual and an automatic operation for assigning macros to desired functions of the ASIC to be produced. See, e.g., '432 patent at 9:14-18; 13:5-7; 13:28-31.

## G. Claim 13: Element [6]

| Claim Language | Ricoh's Construction | Defendants' Construction |
|---|---|---|
| [6] selecting from said stored data for each of the specified definitions a corresponding integrated circuit hardware cell for performing the desired function of the application specific integrated circuit, said step of selecting a hardware cell comprising applying to the specified definition of the action or condition to be performed, a set of cell selection rules stored in said expert system knowledge base and generating for the selected integrated circuit hardware cells, a netlist defining the hardware cells which are needed to perform the desired function of the integrated circuit and the interconnection requirements therefor. | Selecting from the plurality of hardware cells in the hardware cell library a hardware cell for performing the desired function of the desired ASIC through application of the rules; and generating a netlist that identifies the hardware cells needed to perform the function of the desired ASIC and the necessary parameters for connecting the respective inputs and outputs of each hardware cell, the netlist is passed to the next subsequent step in the process for manufacturing the desired ASIC.<br><br>("netlist"= a description of the hardware components (and their interconnections) needed to manufacture the ASIC as used by subsequent processes, e.g., mask development, foundry, etc.) | N. "selecting from said stored data for each of the specified definitions a corresponding integrated circuit hardware cell for performing the desired function of the application specific integrated circuit" -- mapping the specified stored definitions for each logical step and decision represented in the flowchart to a corresponding stored hardware cell description.<br><br>O. "said step of selecting a hardware cell comprising applying to the specified definition of the action or condition to be performed, a set of cell selection rules stored in said expert system knowledge base" -- the mapping of the specified definitions to the stored hardware cell descriptions must be performed by an expert system having an inference engine for selectively applying a set of rules, each rule having an antecedent portion (IF) and a consequent portion (THEN), embodying the knowledge of expert designers for application specific integrated circuits, which enables the expert system to map the specified stored definitions for each logical step and decision represented in the flowchart to a corresponding stored hardware cell description.<br><br>P. "Netlist" -- a structural description that includes a custom controller type hardware cell and all other hardware cells required to implement the application specific integrated circuit's operations and any necessary interconnections including the necessary control and data path information for connecting the hardware cells and the controller. |

| Claim Language | Ricoh's Construction | Defendants' Construction |
|---|---|---|
| | | Q. "generating for the selected integrated circuit hardware cells, a netlist defining the hardware cells which are needed to perform the desired function of the integrated circuit" -- producing a list of the needed hardware cells by eliminating any mapped hardware cells that are redundant or otherwise unnecessary and producing a custom controller type hardware cell for providing the needed control for those other hardware cells and<br><br>R. "generating …interconnection requirements therefor" -- producing the necessary structural control paths and data paths for the needed hardware cells and the custom controller. |

**1. Ricoh's Construction**

This claim element is directed to the step of selecting a hardware cell for performing a desired function of the ASIC to be produced. Ricoh incorporates the definitions (and the bases therefor) for the terms "hardware cell" and "rules," as set forth above.[37] First, the term "netlist" should be defined as: "a description of the hardware components (and their interconnections) needed to manufacture the ASIC as used by subsequent processes, e.g., mask development, foundry, etc."

Ricoh's definition of "netlist" is supported by the '432 patent specification. The '432 patent, for example, teaches: "The list of hardware cells and their interconnection requirements may be represented in the form of a netlist." '432 patent at 2:42-44. The '432 patent further teaches:

[37] See Section V.C.1, supra pp. 24-25 and Section V.D.1, supra pp. 27-28, respectively.

> The netlist is a list which identifies each block in the circuit and the interconnections between the respective inputs and outputs of each block. The netlist provides all the necessary information required to produce the integrated circuit.

Id. at 5:35-40 (emphasis added).[38]

Consistent with the teachings of the '432 patent, the proper definition of the term "netlist" should be: "a description of the hardware components (and their interconnections) needed to manufacture the ASIC as used by subsequent processes, e.g., mask development, foundry, etc."

Claim element [6] initially recites the "selecting" step as: "selecting from said stored data for each of the specified definitions a corresponding integrated circuit hardware cell for performing the desired function of the application specific integrated circuit." Given the proper interpretation of claim element [2] ("storing data describing a set of available integrated circuit hardware cells") as discussed above,[39] this initial clause simply refers to the process step of selecting hardware cells from those stored in the hardware cell library that can be used to implement the desired functions of the ASIC to be produced. As an illustration, for example, the '432 patent describes a preferred embodiment which uses a Cell Selector "for selecting a set of optimum cells from the cell library 34 to implement a VLSI system." '432 patent at 8:21-23.

The remaining clause of claim element [6] more specifically describes the "selecting" step as having the substeps of "applying" a set of cell selection rules and "generating" a netlist:

> said step of selecting a hardware cell comprising[:] [(1)] applying . . . a set of cell selection rules . . . and [(2)] generating . . . a netlist defining the hardware cells which are needed to perform the desired function of the integrated circuit and the interconnection requirements therefor.

'432 patent at 16:56-65 (emphasis added).

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[38] See also id. at 5:40-46 ("Computer-aided design systems for cell placement and routing are commercially available which will receive netlist data as input and will lay out the respective cells in the chip, generate the necessary routing, and produce mask data which can be directly used by a chip foundry in the fabrication of integrated circuits." (emphasis added)).

[39] See Section V.C.1, supra pp. 24-25.

As illustrated in an exemplary embodiment of the '432 patent, the "applying" substep can be seen from the description:

> The knowledge base of Cell Selector 32 contains information (rules) relating to:
>
> (1) selection of macros
>
> (2) merging two macros
>
> (3) mapping of macros to cells
>
> (4) merging two cells
>
> (5) error diagnostics
>
> The above information is stored in the knowledge base 35 as rules.
>
> Cell List Generation
>
> FIG. 9 shows the cell list generation steps. . . . Rules of the following type are applied during this stage.
>
> map arguments to data paths
>
> map actions to macros
>
> connect these blocks
>
> Rules also provide for optimization and error diagnostics at this level.
>
> The cell selector maps the blocks to cells selected from the cell library 34. It selects an optimum cell for a block. This involves the formulation of rules for selecting appropriate cells from the cell library.

'432 patent at 8:65 to 9:24 (emphasis added).

The '432 patent further describes an exemplary implementation of an embodiment of the invention (beginning at column 12, line 36), which involves the design and production of an ASIC for use as a vending machine controller. The '432 patent describes the application of a variety of rules to the "macros" to achieve an optimum set of hardware components and their corresponding connections ("interconnections") as used to implement the desired functions of the ASIC:

> The PSCS program 30 maps each of the macros used in the flowchart of FIG. 10 to the corresponding hardware components results in the generation of the hardware blocks shown in FIG. 12. In generating the illustrated blocks, the PSCS program 30 relied upon rules 1 and 2 of the above listed example rules.

> FIG. 13 illustrates the interconnection of the blocks of FIG. 12 with data paths and control paths. Rule 3 was used by the data/control path synthesizer program 31 in mapping the data and control paths.
>
> FIG. 14 shows the result of optimizing the circuit by applying rule 4 to eliminate redundant registers. As a result of application of this rule, the registers R2, R3, R7, R8, and R9 in FIG. 13 were removed. FIG. 15 shows the block diagram after further optimization in which redundant comparators are consolidated. This optimization is achieved in the PSCS program 30 by application of rule 5.

'432 patent at 13:48-66 (emphasis added).

The '432 patent, through its description of an embodiment and exemplary implementation of the invention, illustrates some preferred operations of the "applying" substep in the context of selection of hardware cells. The completion of the "applying" substep results in the performance of the "generating" substep, which may be best seen from the description of the vending machine controller implementation in the '432 patent:

> Having now defined the system controller block, the other necessary hardware blocks and the data and control paths for the integrated circuit, the PSCS program 30 now generates a netlist 15 defining these hardware components and their interconnection requirements. From this netlist the mask data for producing the integrated circuit can be directly produced using available VLSI CAD tools.

'432 patent at 13:67 to 14:6 (emphasis added).

From the proper interpretation of the term "netlist" and the plain reading of the '432 patent specification, as discussed above, the proper definition of claim element [6] should be:

> Selecting from the plurality of hardware cells in the hardware cell library a hardware cell for performing the desired function of the desired ASIC through application of the rules; and generating a netlist that identifies the hardware cells needed to perform the function of the desired ASIC and the necessary parameters for connecting the respective inputs and outputs of each hardware cell, the netlist is passed to the next subsequent step in the process for manufacturing the desired ASIC.

For at least these reasons, Ricoh's proposed construction should be adopted.

**2. Defendants' Construction**

As a preliminary matter, Defendants' construction improperly rewrites the claim language to include an additional independent step: "generating for the selected integrated circuit hardware cells, . . . ."[40] That Defendants' construction is in error is distinctly evident from a plain reading of the claim language itself. Claim 13, as amended to its final form and issued, includes the "generating" substep as part of the "selecting" step (claim element [6]). A plain reading of the "generating" substep in context shows an intent by the patentee to list the substeps comprising the "selecting" step as including both "applying" and "generating" substeps. Additionally, it is noted that the last two claim elements (i.e., the "specifying" step (claim element [5]) and the "selecting" step (claim element [6])) are separated by a semicolon and the conjunction "and." Traditionally in patent claim drafting, and consistently for all claims in the '432 patent, this format (i.e., " ; and") is used after the penultimate claim element of any claim listing more than one claim element. Thus, from a plain reading of the "selecting" step (claim element [6]), consistent with the traditional rules of patent claim drafting, the Court can only conclude that the "generating" substep has always been intended to be a substep forming a part of the "selecting" step.[41]

Defendants' proposed construction of the phrase "selecting from said stored data . . . of the application specific integrated circuit"[42] is improper primarily for its adoption of previous proposed constructions that attempt to limit the claim to one of the preferred embodiments disclosed in the '432 patent (i.e., the use of a flowchart input specification). Ricoh's position in opposition was provided in detail above.[43] For at least the reasons set forth previously, Defendants' proposed construction is improper.

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[40] JCC Statement, Exhibit A, at 19 (clause "Q").

[41] The only rationale Ricoh can imagine for Defendants' hollow attempt to separate the "generating" substep is Defendants' belief that doing so will support some non-infringement theory later at trial.

[42] See JCC Statement, Exhibit A, at 16 (clause "N").

[43] See, e.g., Section V.B.2.a, supra pp. 17-18; V.E.2, supra pp. 34-37.

Defendants' proposed construction of the phrase "said step of selecting a hardware cell . . . in said expert system knowledge base"[44] is improper primarily for its adoption of previous proposed constructions that attempt to limit the claim to one of the preferred embodiments disclosed in the '432 patent (i.e., the use of an expert system and rules having an IF-THEN format). Ricoh's position in opposition to such improper contentions was provided in detail above.[45] For at least the reasons set forth previously, Defendants' proposed construction is improper.

Defendants' construction of the term "netlist" to mean "a structural description that includes a custom controller . . . [as well as] the necessary control and data path information for connecting the hardware cells and the controller"[46] is improper. From this definition, it is evident that Defendants are (again) attempting to restrict the definition of a claim term to the details of a preferred embodiment disclosed in the '432 patent. In a preferred embodiment, for example, the '432 patent describes the use of netlist 15 that "includes a custom generated system controller, all other hardware cells required to implement the necessary operations, and interconnection information for connecting the hardware cells and the system controller." '432 patent at 4:39-43.[47]

Defendants' construction is thus improper because it attempts to limit the construction to a preferred embodiment merely because it is (allegedly) the only embodiment disclosed. SRI Int'l, 775 F.2d at 1121 n.14 ("That a specification describes only one embodiment does not require that each claim be limited to that one embodiment.");

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[44] See JCC Statement, Exhibit A, at 16-17 (clause "O").

[45] See, e.g., Section V.E.2, supra pp. 34-37.

[46] See JCC Statement, Exhibit A, at 19 (clause "P").

[47] See also id. at 5:31-36 ("Referring again to FIG. 3, the cells selected by the cell selector 32, the controller information generated by the controller generator 33 and the data and control paths generated by the data/control path synthesizer 31 are all utilized by the PSCS program 30 to generate the netlist 15.").

see also Tex. Digital Sys., 308 F.3d at 1204. Defendants' construction is also improper because it adds limitations (e.g., "custom controller" and "control and data path") to the claim that are expressly recited in other claims.[48] See SRI Int'l, 775 F.2d at 1122.

For at least these reasons, Defendants' proposed construction of claim element [6] is improper and Ricoh's proposed construction should be adopted.

### H. Claim 14

| Claim Language | Ricoh's Construction | Defendants' Construction |
|---|---|---|
| 14. A process as defined in claim 13, including generating from the netlist the mask data required to produce an integrated circuit having the desired function. | The process of claim 13, including producing from the netlist of hardware cells to be included in the designed ASIC mask data which can be directly used by a chip foundry in the fabrication of the ASIC. | S. "generating from the netlist the mask data required to produce an integrated circuit having the desired function" -- producing, from the structural netlist, the detailed layout level geometrical information required for manufacturing the set of photomasks that are used by the processes that directly manufacture the application specific integrated circuit. |

#### 1. Ricoh's Construction

Claim 14 is directed to the generation of mask data used to produce the ASIC to be manufactured. Ricoh incorporates the definitions (and bases therefor) discussed above with respect to claim 13. In connection with the manufacture of chips, the '432 patent describes use of a "physical chip layout level description which describes the actual topological characteristics of the integrated circuit chip." '432 patent at 1:38-42. The '432 patent teaches that "[t]his

[48] See, e.g., '432 patent claim 10 ("The system as defined in claim 9 additionally including control generator means for generating a controller and control paths for the hardware cells selected by said cell selection means."); claim 15 ("A process as defined in claim 13 including the further step of generating data paths for the selected integrated circuit hardware cells."); claim 17 ("A process as defined in claim 16 including the further step of generating control paths for the selected integrated circuit hardware cells.").

physical chip layout level description provides the mask data needed for fabricating the chip." Id. at 1:42-44; see also id. at Fig. 1c & 3:68 to 4:4 ("FIG. 1c illustrates a physical layout level representation of an integrated circuit design, which provides the detailed mask data necessary to actually manufacture the devices and conductors which together comprise integrated circuit.").

In accordance with a preferred embodiment, the '432 patent teaches the use of computer-aided design systems "which will receive netlist data as input and will lay out the respective cells in the chip, generate the necessary routing, and produce mask data which can be directly used by a chip foundry in the fabrication of integrated circuits." '432 patent at 5:40-46.

Ricoh's definition of this claim (i.e., "producing from the netlist of hardware cells to be included in the designed ASIC mask data which can be directly used by a chip foundry in the fabrication of the ASIC") is therefore consistent with the '432 patent specification.

For at least these reasons, Ricoh's proposed construction should be adopted.

**2. Defendants' Construction**

Defendants' proposed construction of claim 14 is improper primarily for its adoption of previous proposed constructions that attempt to limit the definition of the term "netlist." Ricoh's position in opposition was provided in detail above.[49]

For at least the reasons set forth previously, Defendants' proposed construction of claim 14 is improper and Ricoh's proposed construction should be adopted.

**I. Claim 15**

| Claim Language | Ricoh's Construction | Defendants' Construction |
|---|---|---|
| 15. A process as defined in claim 13 including the further step of generating data paths for the selected integrated circuit | The process of claim 13, including producing signal lines for carrying data to the hardware cells. | T. "generating data paths for the selected integrated circuit hardware cells" -- producing the necessary structural descriptions of the data paths for the mapped |

[49] See, e.g., Section V.G.2, supra pp. 45-47.

| Claim Language | Ricoh's Construction | Defendants' Construction |
|---|---|---|
| hardware cells. | | hardware cells. |

**1. Ricoh's Construction**

Claim 15 is directed to the step of producing data signal lines between the hardware cells selected for implementation in the ASIC to be produced. Ricoh incorporates the definitions (and bases therefor) discussed above with respect to claim 13. In particular, this claim should be defined as: "producing signal lines for carrying data to the hardware cells."

Ricoh's definition is supported by the '432 patent specification. The '432 patent teaches that "[t]he system also generates data paths among the selected hardware cells." '432 patent at 2:39-40. The '432 patent further states, with respect to the hardware blocks shown in Fig. 1b, "lines interconnecting the blocks represent paths for the flow of data or control signals between the blocks." Id. at 3:60-65. Other illustrations of the data paths can be found in the '432 patent, for example, in Fig. 13 (showing the interconnections between the hardware blocks selected in Fig. 12). Consistent with these teachings of the '432 patent, claim 15 is properly defined as noted above.

For at least these reasons, Ricoh's proposed construction should be adopted.

**2. Defendants' Construction**

Defendants' proposed construction defines claim 15 as the step of: "producing the necessary structural descriptions of the data paths for the mapped hardware cells." To the extent that this definition intends to imply that the term "structural descriptions" does not cover the "signal lines for carrying data to the hardware cells," as set forth in Ricoh's proposed construction, Defendants' construction is improper. As noted above, the '432 patent specification clearly shows that the "data paths" described in the preferred embodiments of the '432 patent include at least the signal lines carrying data between hardware cells. Thus, to the extent that the use of the term "structural descriptions" in Defendants' construction seeks to

exclude coverage of one of the preferred embodiments of the '432 patent, Defendants' construction is improper. Zimmer, 2004 U.S. App. LEXIS 10598, at *11.

For at least the reasons given above, Defendants' proposed construction of claim 15 is improper and Ricoh's proposed construction should be adopted.

### J. Claim 16

| Claim Language | Ricoh's Construction | Defendants' Construction |
|---|---|---|
| 16. A process as defined in claim 15 wherein said step of generating data paths comprises applying to the selected cells a set of data path rules stored in a knowledge base and generating the data paths therefrom. | The process of claim 15, wherein the step of producing signal lines for carrying data comprises applying rules, which are placed in computer memory, to produce the signal lines for carrying data to the hardware cells. | U. "said step of generating data paths comprises applying to the selected cells a set of data path rules stored in a knowledge base and generating the data paths therefrom" -- the generating step must be performed by at least an expert system having an inference engine for selectively applying a set of rules, each having an antecedent portion (IF) and a consequent portion (THEN), embodying the knowledge of expert designers for application specific integrated circuits, which enables the expert system to produce the necessary data paths for the mapped hardware cells. |

#### 1. Ricoh's Construction

Claim 16 is directed to the generation of data paths by applying rules stored in a knowledge base. Ricoh incorporates the definitions (and bases therefor) discussed above with respect to claims 13 and 15. In a preferred embodiment, the '432 patent specification describes the use of "a data and control path synthesizer module 31, which is a knowledge based system for data and control path synthesis." '432 patent at 4:64-66. The knowledge based system applies rules to map or generate the data and control paths. Id. at 13:55-58 ("FIG. 13 illustrates the interconnection of the blocks of FIG. 12 with data paths and control paths. Rule 3 was used by the data/control path synthesizer program 31 in mapping the data and control paths.").

The '432 patent thus supports Ricoh's contention that claim 16 should be defined as: "applying rules, which are placed in computer memory, to produce the signal lines for carrying data to the hardware cells."

For at least these reasons, Ricoh's proposed construction should be adopted.

### 2. Defendants' Construction

Defendants' proposed construction of claim 16 is improper primarily for its adoption of previous proposed constructions that attempt to limit the claim to the details of one of the preferred embodiments disclosed in the '432 patent (i.e., the use of an expert system and rules having an IF-THEN format). Ricoh's position in opposition was provided in detail above.[50]

For at least the reasons given above, Defendants' proposed construction of claim 16 is improper and Ricoh's proposed construction should be adopted.

## K. Claim 17

| Claim Language | Ricoh's Construction | Defendants' Construction |
|---|---|---|
| 17. A process as defined in claim 16 including the further step of generating control paths for the selected integrated circuit hardware cells. | The process of claim 16, including producing signal lines for carrying control signals to the hardware cells. | V. "generating control paths for the selected integrated circuit hardware cells" -- producing the necessary structural descriptions of the control paths for the selected hardware cells. |

### 1. Ricoh's Construction

Claim 17 is directed to the step of producing control signal lines for control of the hardware cells selected for implementation in the ASIC to be produced. Ricoh incorporates the definitions (and bases therefor) discussed above with respect to claims 13, 15, and 16. In

[50] See, e.g., Section V.E.2, supra pp. 34-37.

particular, this claim element is defined as: "producing signal lines for carrying control signals to the hardware cells."

Ricoh's definition is consistent with (and supported by) the '432 patent specification. The '432 patent teaches that "the present invention generates a system controller and control paths for the selected integrated circuit hardware cells." '432 patent at 2:40-42. As noted above, with respect to claim 15,[51] the '432 patent further states, with respect to the hardware blocks shown in Fig. 1b, "lines interconnecting the blocks represent paths for the flow of data or control signals between the blocks." Id. at 3:60-65. Consistent with these teachings of the '432 patent, claim 17 should be properly defined as noted above.

For at least these reasons, Ricoh's proposed construction should be adopted.

**2. Defendants' Construction**

Much like their proposed construction of claim 15, Defendants' proposed construction of claim 17 uses the term "structural descriptions."[52] To the extent that the use of this term is intended to exclude the "signal lines for carrying control signals to the hardware cells," as set forth in Ricoh's proposed construction, Defendants' construction is improper. As noted above, with respect to claim 15,[53] the '432 patent specification clearly shows that the "control paths" described in the preferred embodiments of the '432 patent include at least the control signal lines to the hardware cells. Thus, to the extent that the use of the term "structural descriptions" in Defendants' construction seeks to exclude coverage of one of the preferred embodiments of the '432 patent, Defendants' construction is improper. Zimmer, 2004 U.S. App. LEXIS 10598, at *11.

[51] See Section V.I.1, supra p. 49.

[52] See JCC Statement, Exhibit A, at 23 (clause "V").

[53] See Section V.I.1, supra p. 49.

For at least the reasons given above, Defendants' proposed construction of claim 17 is improper and Ricoh's proposed construction should be adopted.

## VI. CONCLUSION

Based on the analysis above, Ricoh respectfully requests that the Court adopt the foregoing constructions of claims 13-17 of the '432 patent as proposed by Ricoh.

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